FIG. 1

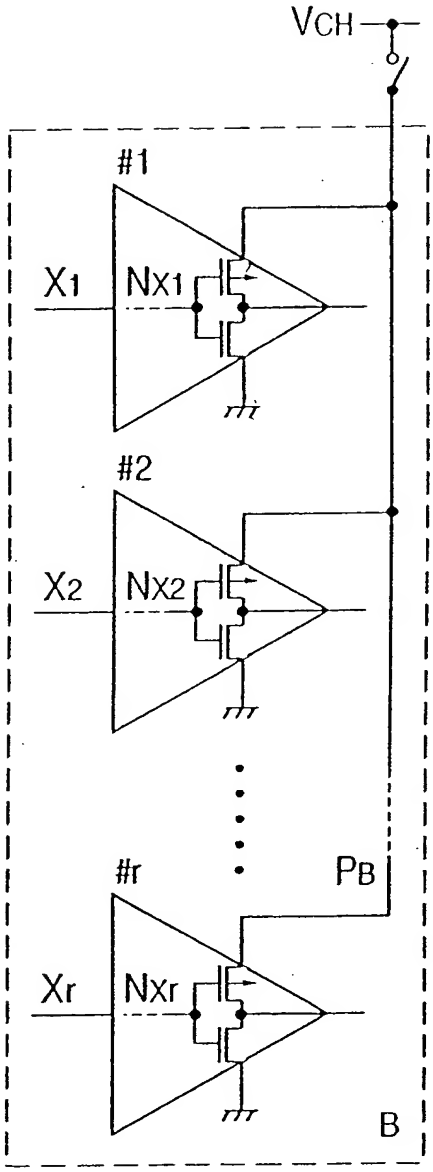


FIG. 2

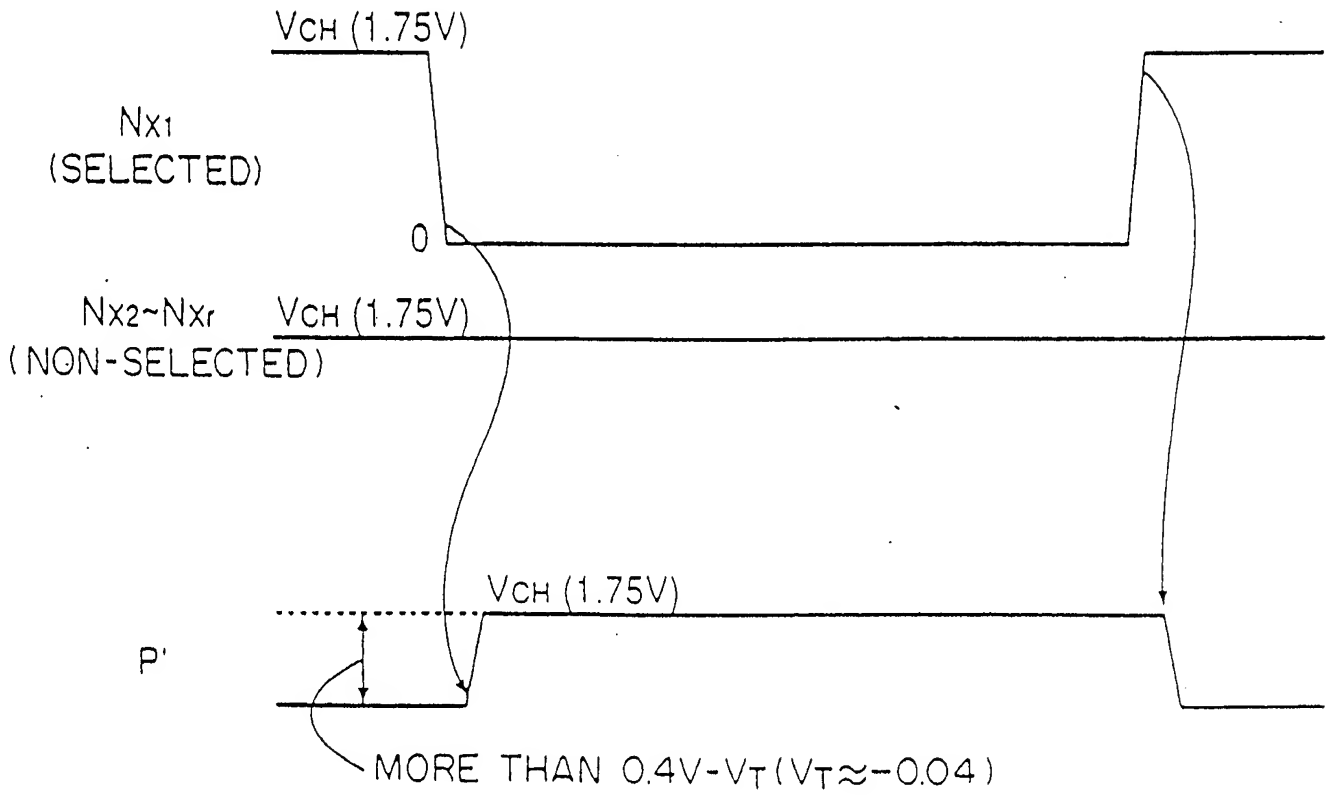

VCH (1.75V)
NX1
(SELECTED)
0
NX2~NXr
(NON-SELECTED)
VCH (1.75V)
VCH (1.75V)
P'
MORE THAN 0.4V-VT (VT≈-0.04)

FIG. 3

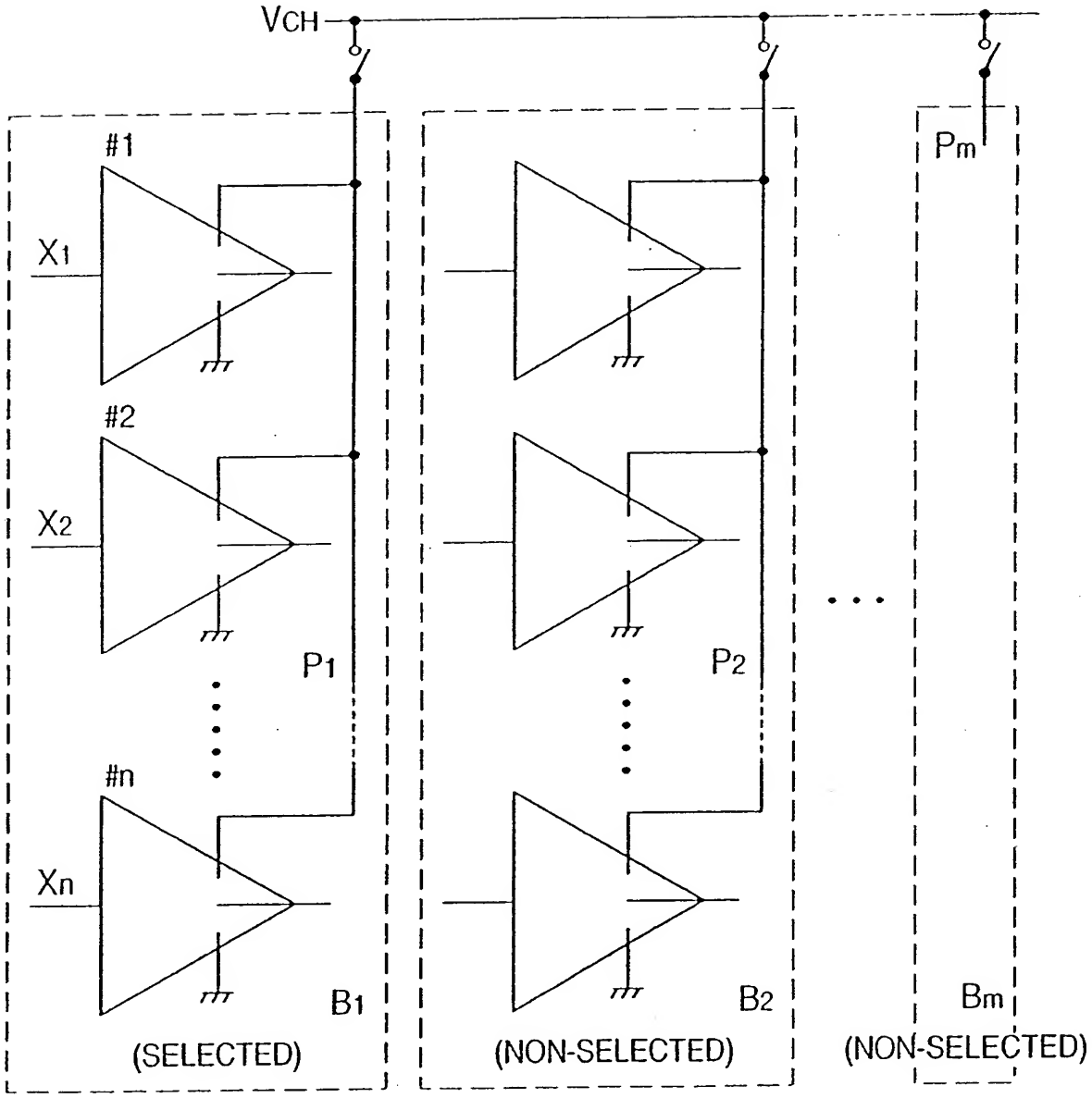

VCH
#1
X1
#2
X2
P1
#n
Xn
B1
(SELECTED)
P2
B2
(NON-SELECTED)
Pm
Bm
(NON-SELECTED)

FIG. 4

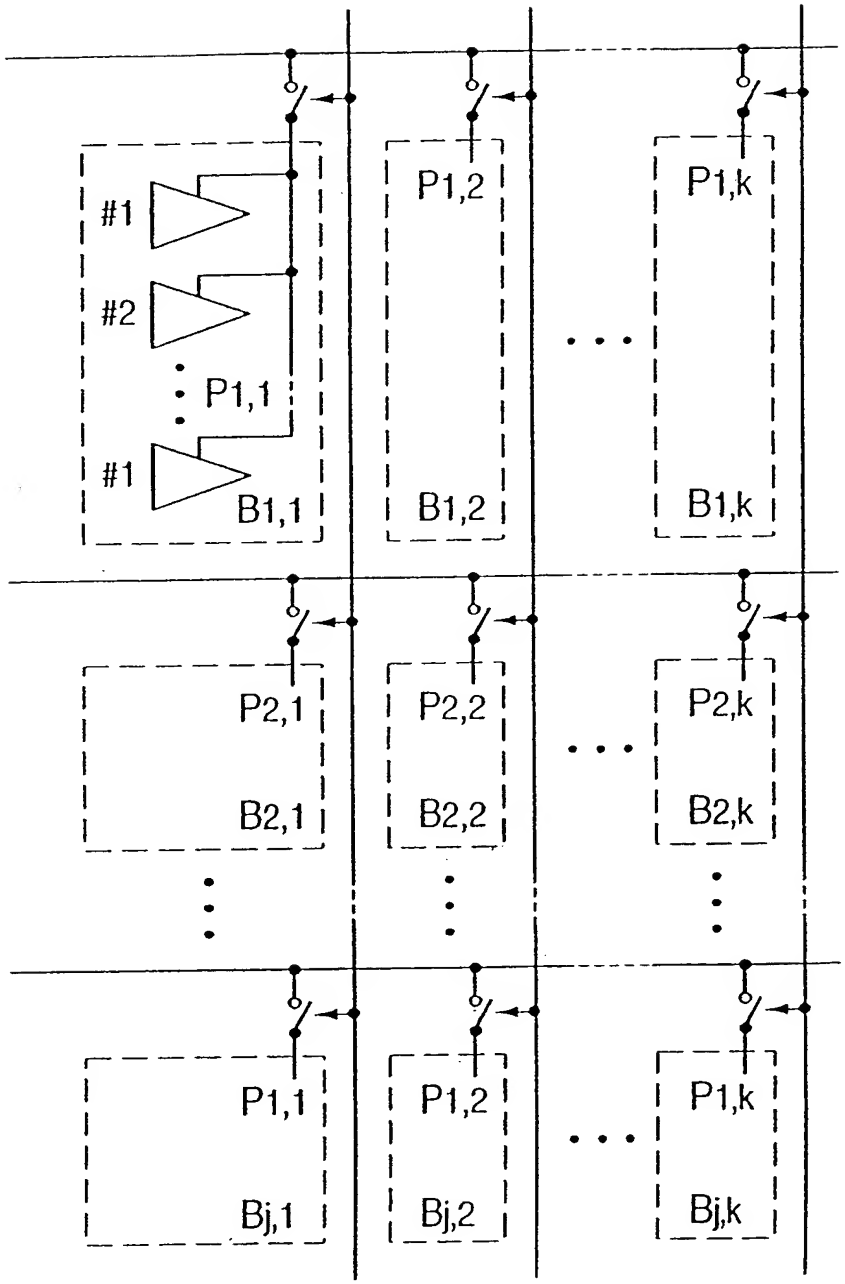

#1
#2
P1,1
#1
B1,1
P1,2
B1,2
P1,k
B1,k
P2,1
B2,1
P2,2
B2,2
P2,k
B2,k
P1,1
Bj,1
P1,2
Bj,2
P1,k
Bj,k

FIG. 5A

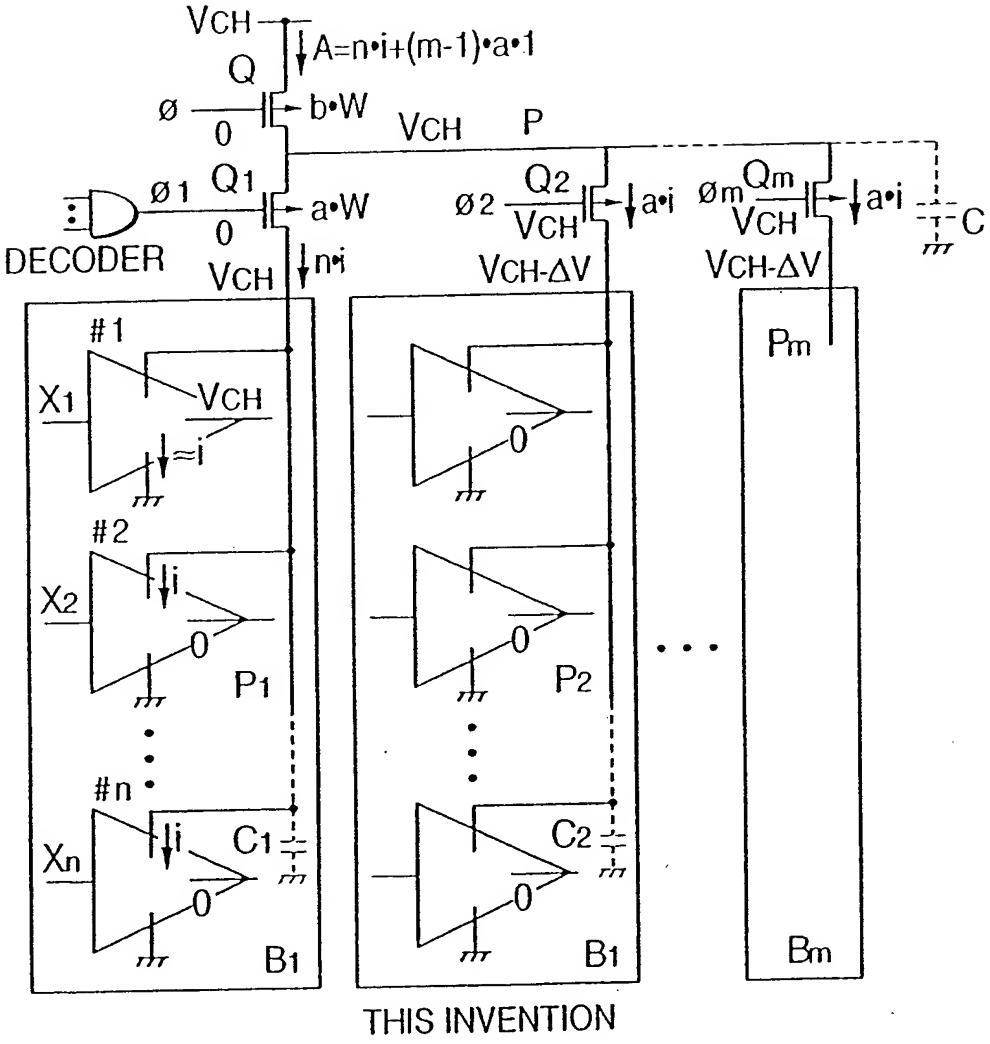

VCH
A=n•i+(m-1)•a•1
Q
ø
0
b•W
VCH
P
ø1
Q1
a•W
0
DECODER
VCH
n•i
ø2
Q2
VCH
a•i
VCH-ΔV
øm
Qm
VCH
a•i
VCH-ΔV
C
#1
X1
VCH
≈i
#2
X2
i
0
P1
P2
Pm
#n
Xn
i
C1
C2
0
B1
B1
Bm
THIS INVENTION

FIG. 5B

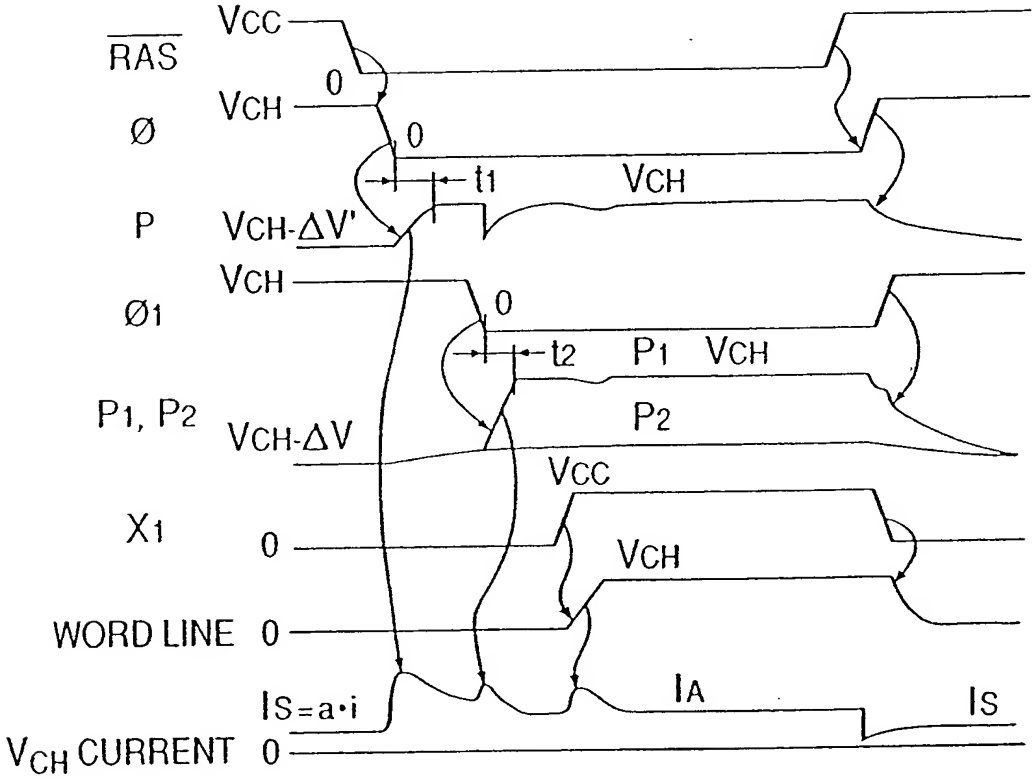

RAS
Ø
P
Ø1
P1, P2
X1
WORD LINE
VCH CURRENT
Vcc
VCH
0
t1
VCH-ΔV'
t2
P1
P2
VCH-ΔV
IS=a·i
IA
IS

FIG. 6

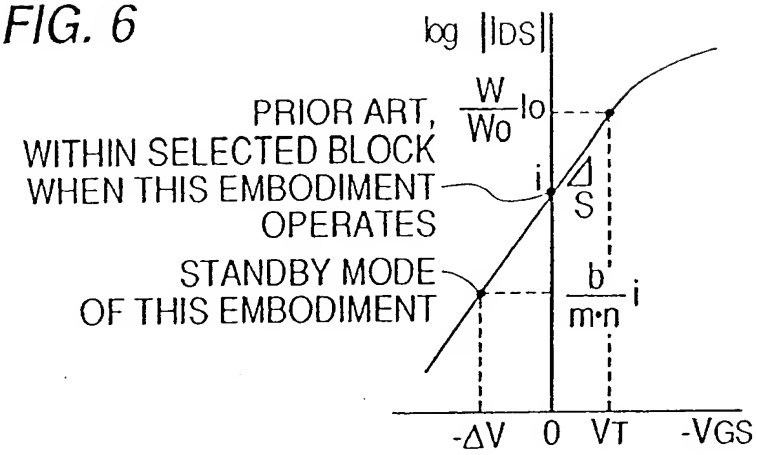

log |IDS|
PRIOR ART,
WITHIN SELECTED BLOCK
WHEN THIS EMBODIMENT
OPERATES
STANDBY MODE
OF THIS EMBODIMENT
W/Wo Io
i
S
b/m·n i
-ΔV
0
VT
-VGS

FIG. 7

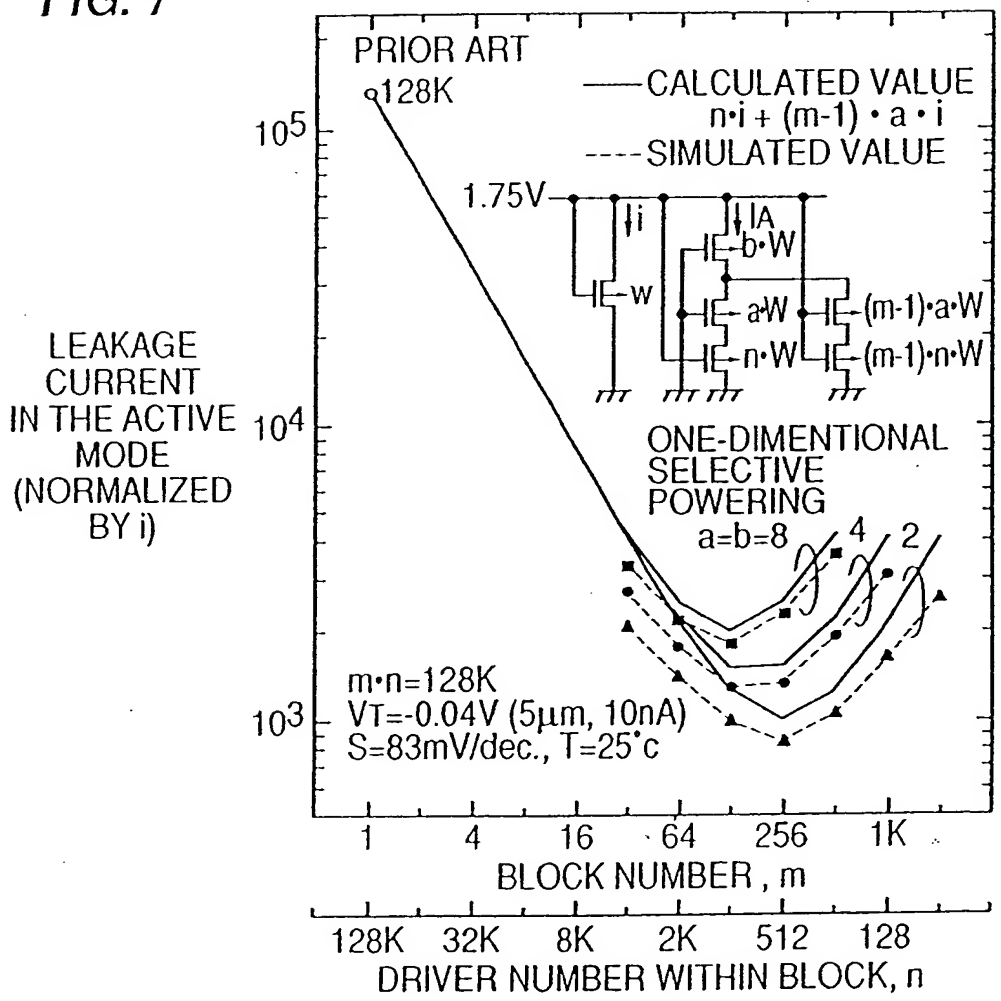

PRIOR ART
128K
CALCULATED VALUE
n·i + (m-1) · a · i
SIMULATED VALUE
1.75V
i
IA
b·W
w
a·W
(m-1)·a·W
n·W
(m-1)·n·W
ONE-DIMENTIONAL
SELECTIVE
POWERING
a=b=8
4
2
m·n=128K
VT=-0.04V (5μm, 10nA)
S=83mV/dec., T=25°c
LEAKAGE
CURRENT
IN THE ACTIVE
MODE
(NORMALIZED
BY i)
10^5
10^4
10^3
1
4
16
64
256
1K
BLOCK NUMBER , m
128K
32K
8K
2K
512
128
DRIVER NUMBER WITHIN BLOCK, n

FIG. 8

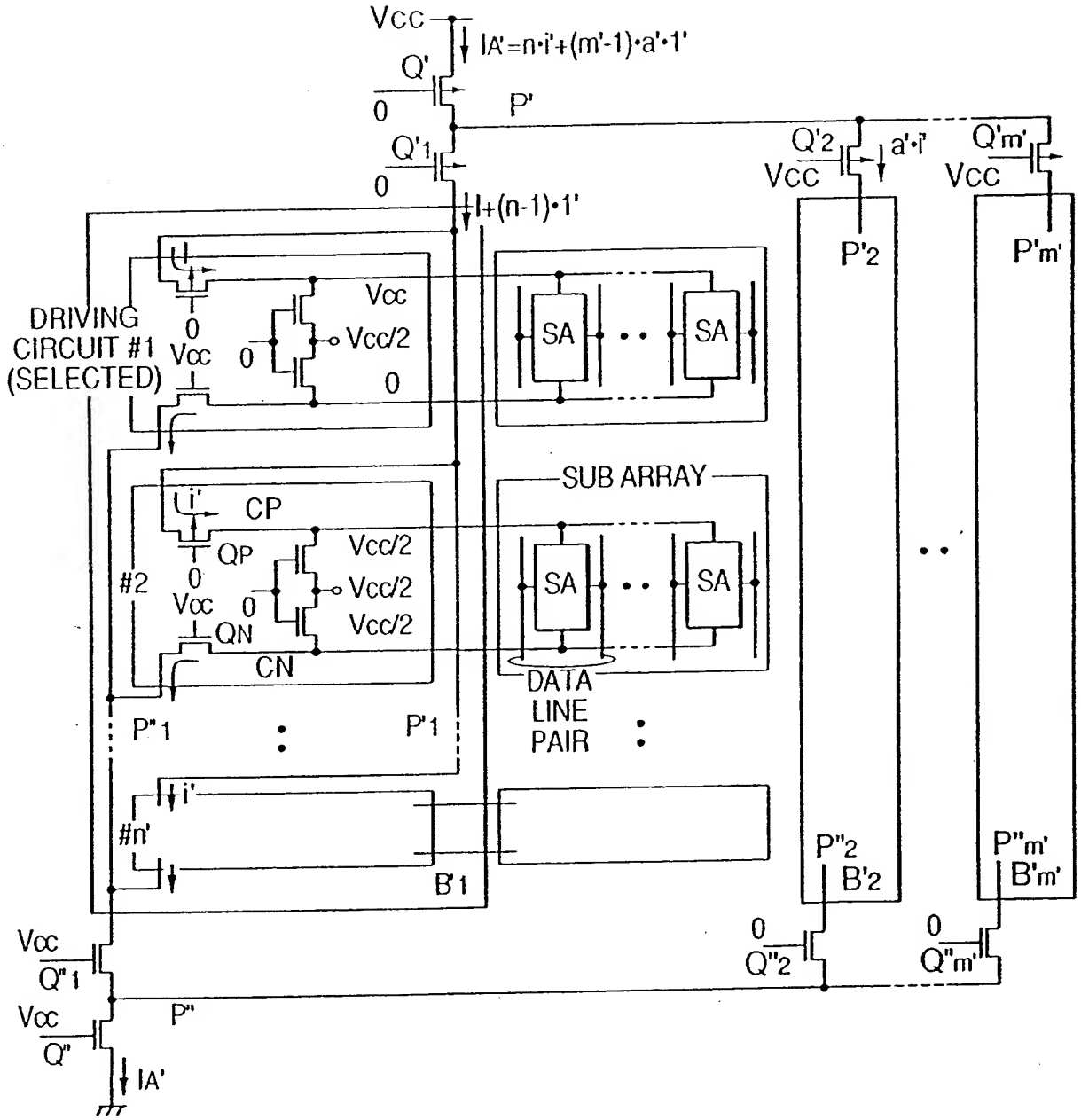

Vcc
IA'=n•i'+(m'-1)•a'•1'
Q'
P'
Q'1
I+(n-1)•1'
Q'2
a'•i'
Q'm'
P'2
P'm'
DRIVING CIRCUIT #1 (SELECTED)
Vcc
Vcc/2
SA
SUB ARRAY
i'
CP
QP
QN
CN
#2
#n'
P"1
P'1
DATA LINE PAIR
B'1
P"2
B'2
P"m'
B'm'
Q"1
Q"
P"
Q"2
Q"m'
IA'

FIG. 9

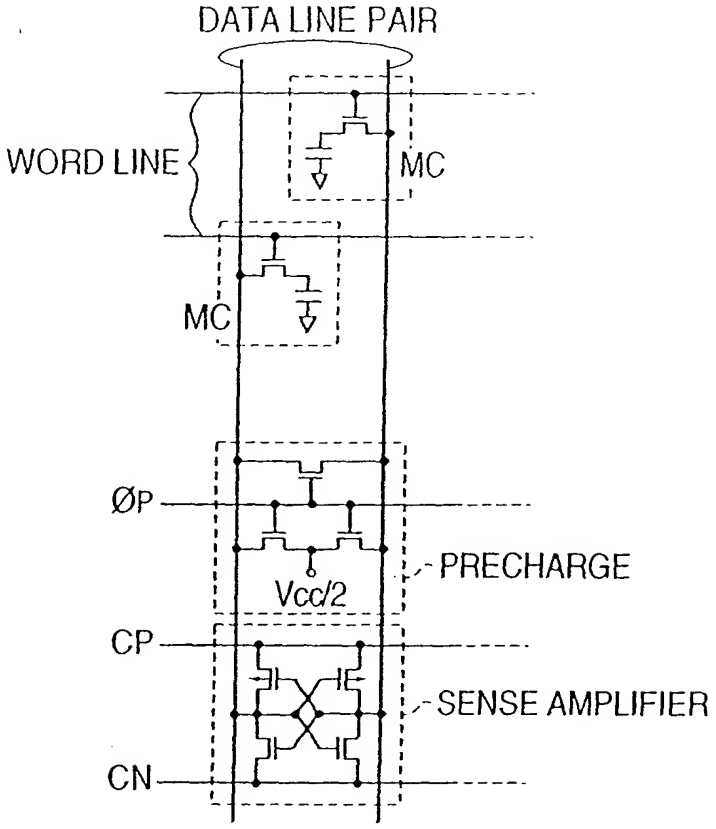

DATA LINE PAIR
WORD LINE
MC
MC
ØP
PRECHARGE
Vcc/2
CP
SENSE AMPLIFIER
CN

FIG. 10

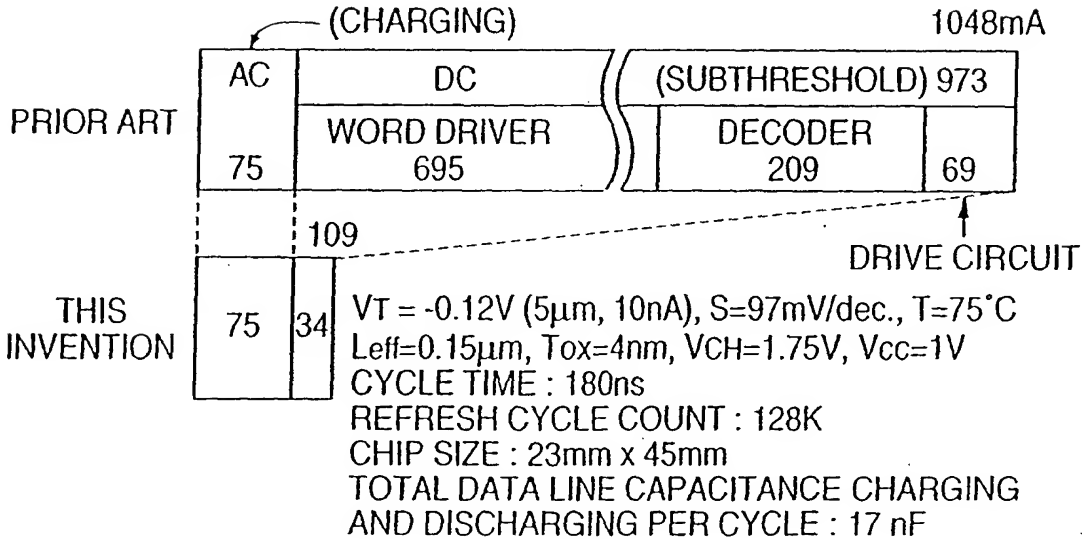

(CHARGING)
1048mA
PRIOR ART
AC
75
DC
WORD DRIVER
695
(SUBTHRESHOLD) 973
DECODER
209
69
109
DRIVE CIRCUIT
THIS INVENTION
75
34
VT = -0.12V (5µm, 10nA), S=97mV/dec., T=75°C
Leff=0.15µm, Tox=4nm, VCH=1.75V, Vcc=1V
CYCLE TIME : 180ns
REFRESH CYCLE COUNT : 128K
CHIP SIZE : 23mm x 45mm
TOTAL DATA LINE CAPACITANCE CHARGING
AND DISCHARGING PER CYCLE : 17 nF

FIG. 11

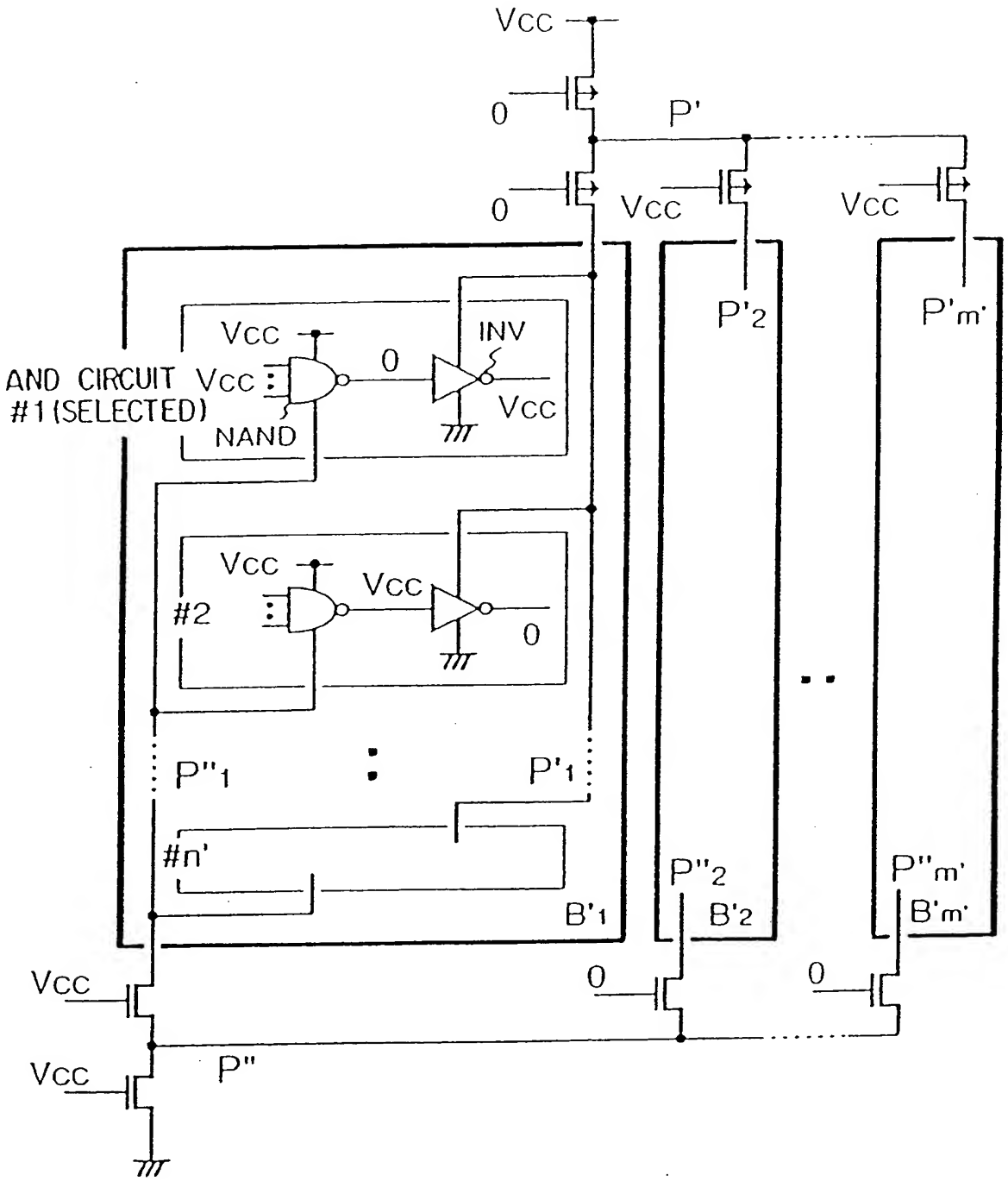

Vcc
0
P'
Vcc
Vcc
P'2
P'm'
INV
AND CIRCUIT
#1 (SELECTED)
NAND
#2
P"1
P'1
#n'
B'1
P"2
B'2
P"m'
B'm'
P"

FIG. 12

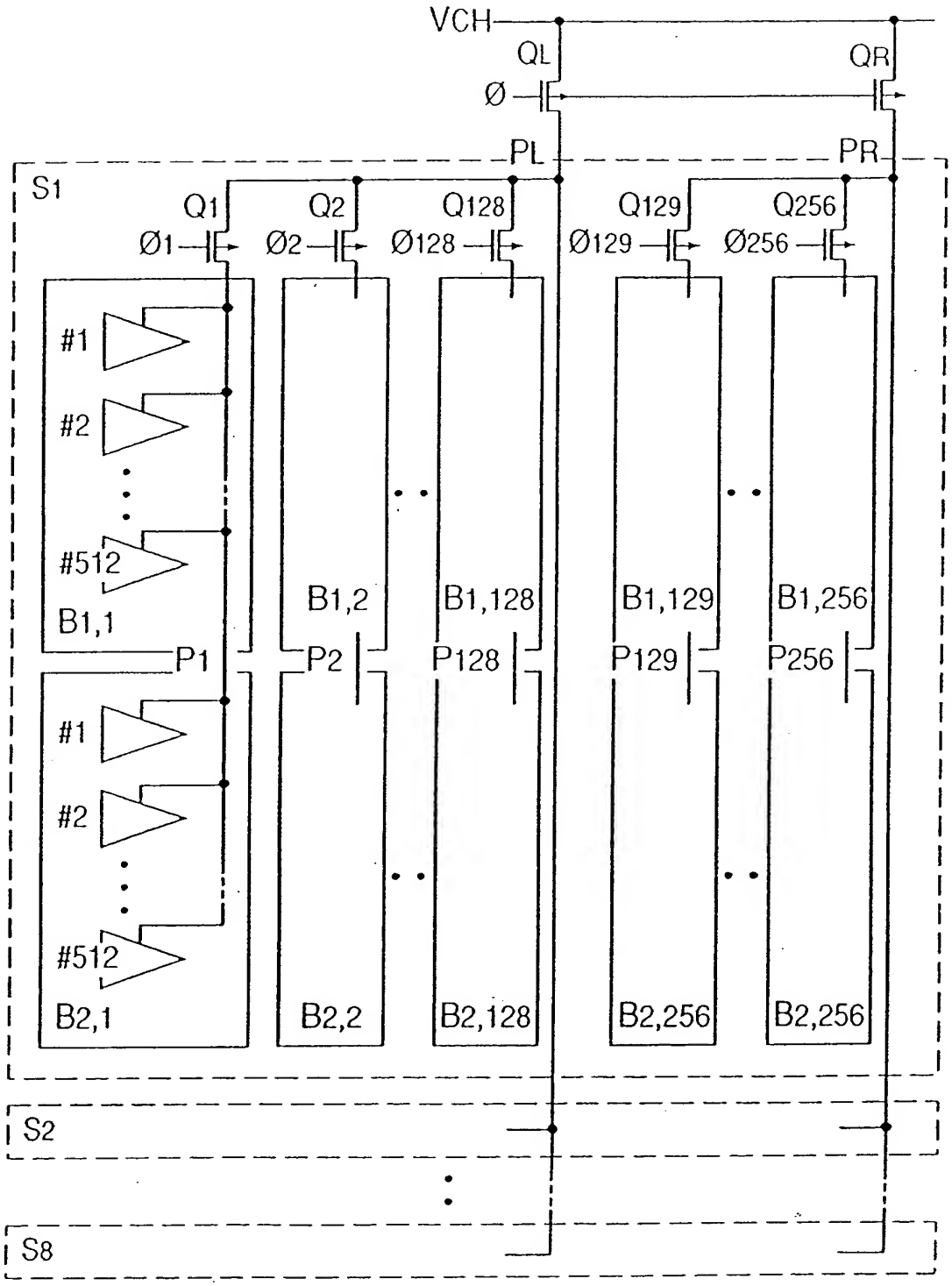

VCH
QL
QR
Ø
PL
PR
S1
Q1
Q2
Q128
Q129
Q256
Ø1
Ø2
Ø128
Ø129
Ø256
#1
#2
#512
B1,1
B1,2
B1,128
B1,129
B1,256
P1
P2
P128
P129
P256
#1
#2
#512
B2,1
B2,2
B2,128
B2,256
B2,256
S2
S8

FIG. 13

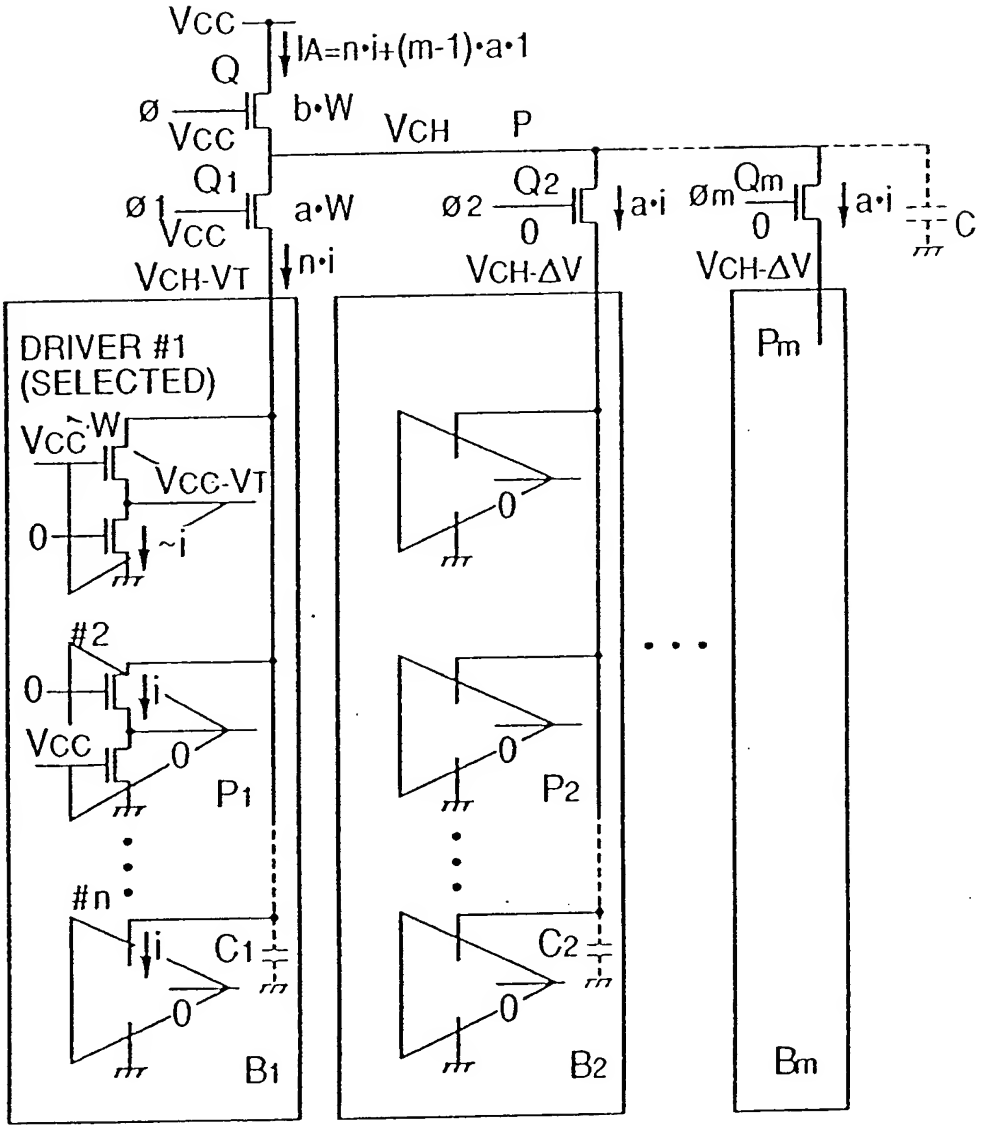

Vcc
IA=n•i+(m-1)•a•1
Q
ø
Vcc
b•W
VCH
P
Q1
ø1
Vcc
a•W
n•i
VCH-VT
Q2
ø2
0
a•i
VCH-ΔV
Qm
øm
0
a•i
VCH-ΔV
C
DRIVER #1
(SELECTED)
Pm
Vcc
W
Vcc-VT
0
~i
#2
0
i
Vcc
0
P1
P2
#n
i
C1
C2
0
B1
B2
Bm

FIG. 14

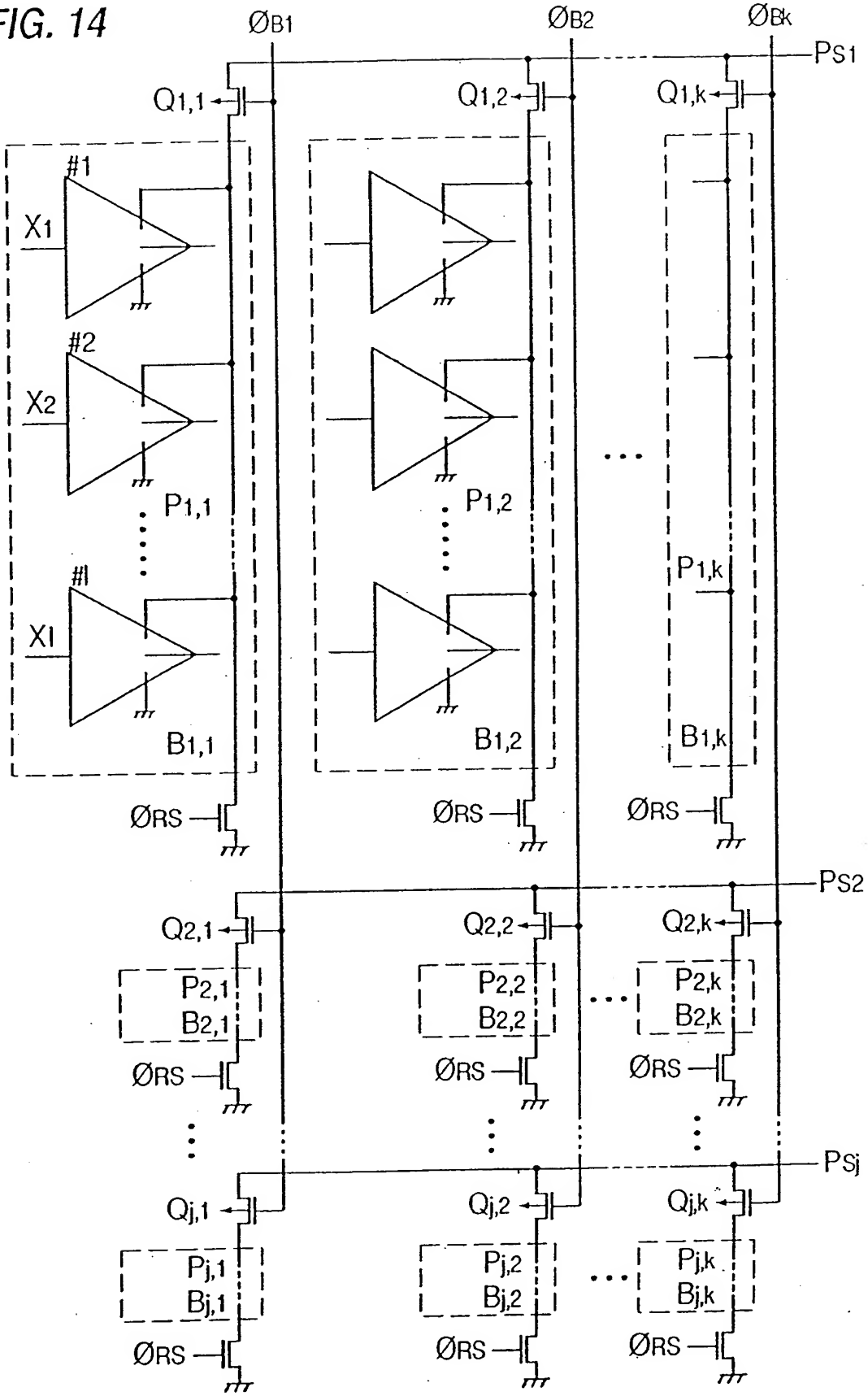

ØB1
ØB2
ØBk
PS1
Q1,1
Q1,2
Q1,k
#1
X1
#2
X2
#I
XI
P1,1
P1,2
P1,k
B1,1
B1,2
B1,k
ØRS
PS2
Q2,1
Q2,2
Q2,k
P2,1
B2,1
P2,2
B2,2
P2,k
B2,k
PSj
Qj,1
Qj,2
Qj,k
Pj,1
Bj,1
Pj,2
Bj,2
Pj,k
Bj,k

FIG. 15

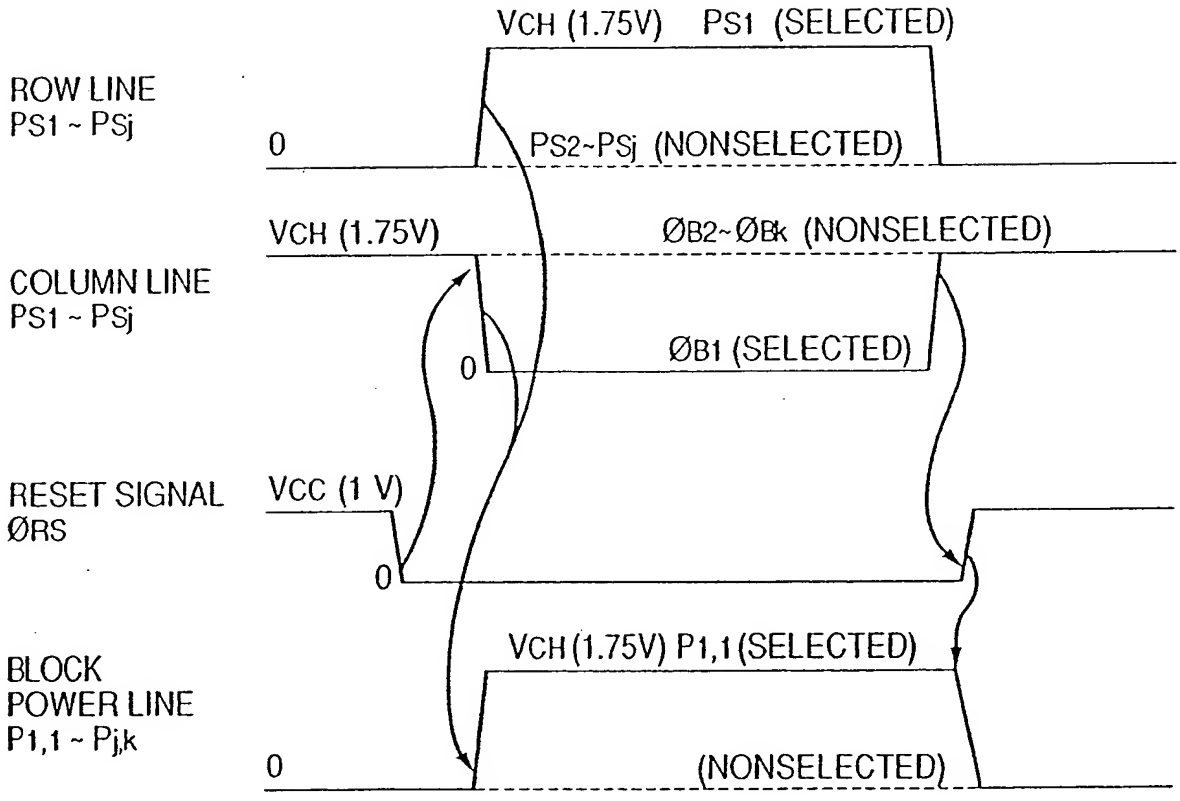

VCH (1.75V) PS1 (SELECTED)
ROW LINE
PS1 ~ PSj
0
PS2~PSj (NONSELECTED)
VCH (1.75V)
ØB2~ØBk (NONSELECTED)
COLUMN LINE
PS1 ~ PSj
ØB1 (SELECTED)
0
RESET SIGNAL
ØRS
VCC (1 V)
0
VCH (1.75V) P1,1 (SELECTED)
BLOCK
POWER LINE
P1,1 ~ Pj,k
0
(NONSELECTED)

FIG. 16A

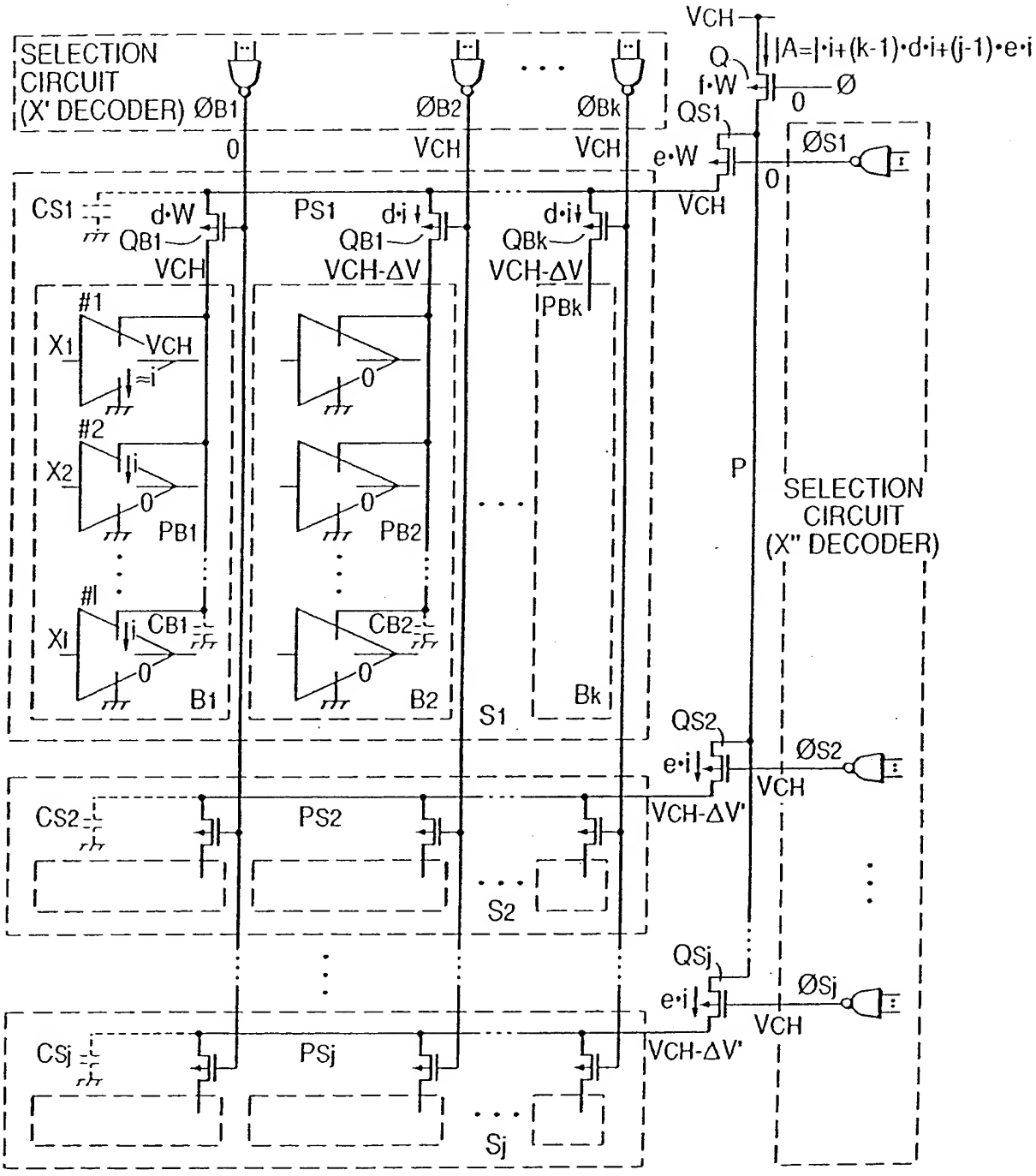

SELECTION CIRCUIT (X' DECODER)
ØB1
ØB2
ØBk
VCH
A=|·i+(k-1)·d·i+(j-1)·e·i
Q
f·W
Ø
QS1
e·W
ØS1
CS1
d·W
QB1
PS1
d·i
QBk
VCH-ΔV
PBk
#1
X1
≈i
#2
X2
i
PB1
PB2
#l
Xl
CB1
CB2
B1
B2
S1
Bk
P
SELECTION CIRCUIT (X" DECODER)
QS2
e·i
ØS2
VCH-ΔV'
CS2
PS2
S2
QSj
ØSj
CSj
PSj
Sj

FIG. 16B

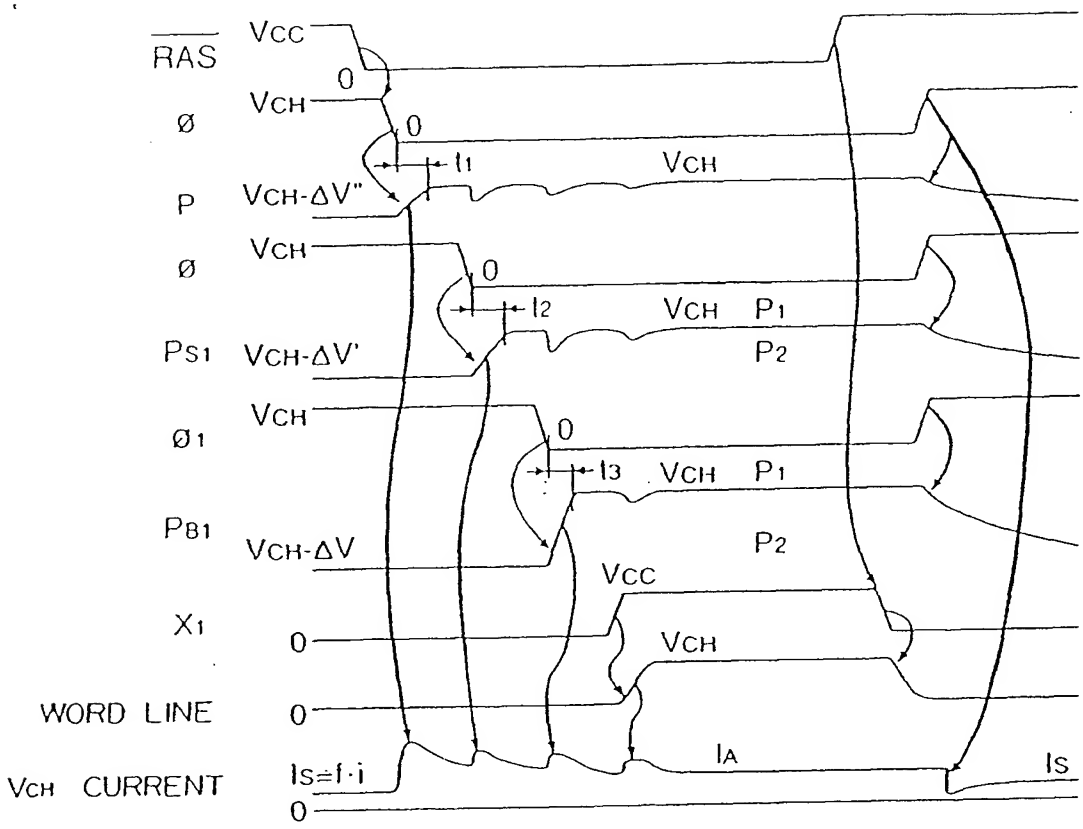


FIG. 17

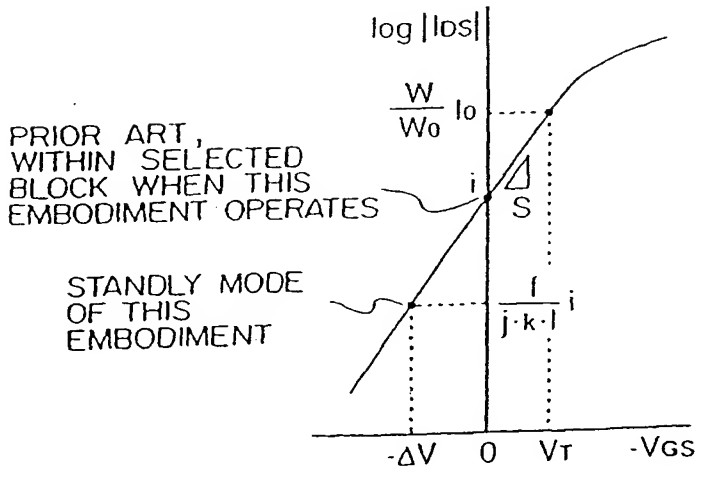


FIG. 18A

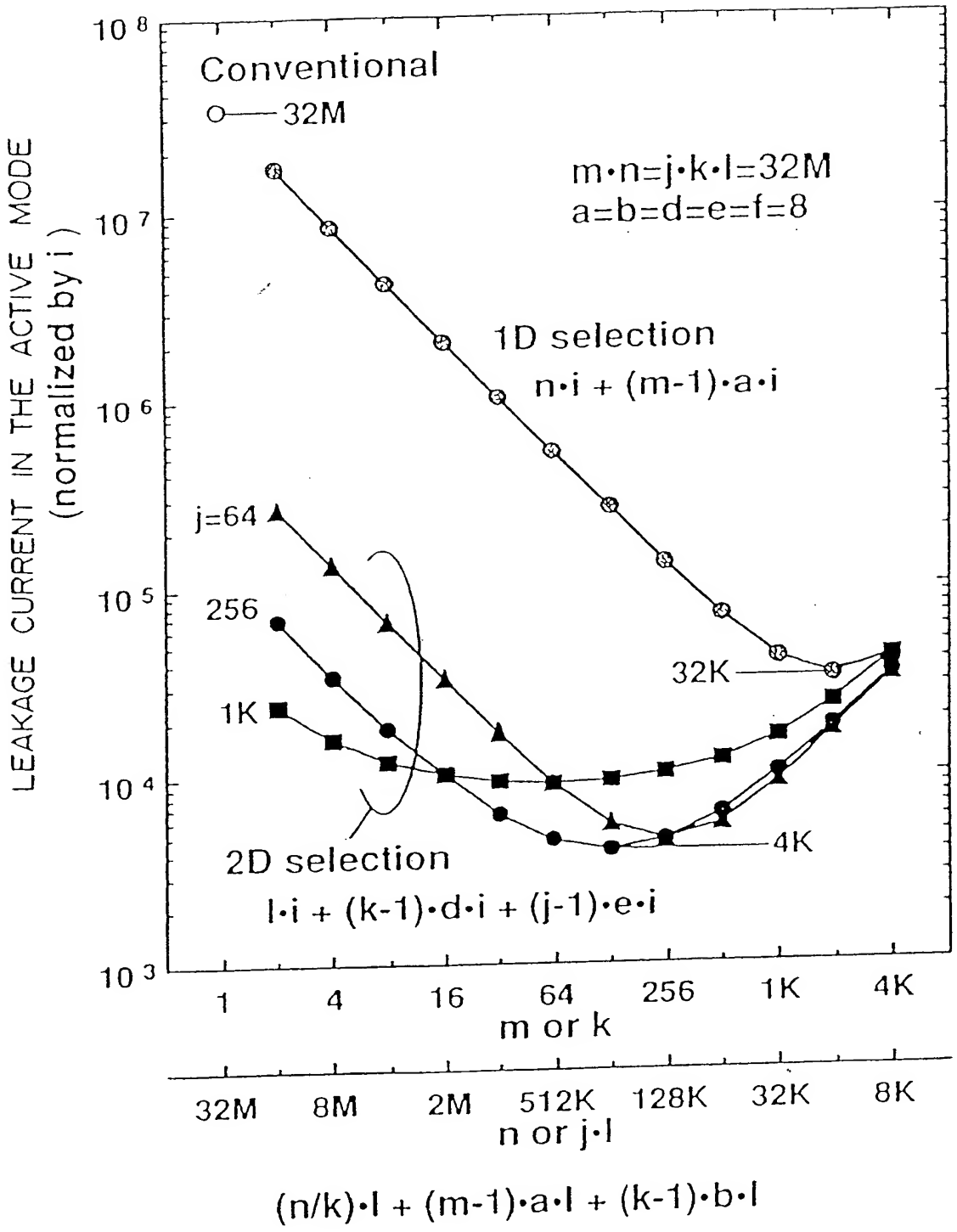

LEAKAGE CURRENT IN THE ACTIVE MODE
(normalized by i)
10 8
10 7
10 6
10 5
10 4
10 3
Conventional
32M
m·n=j·k·l=32M
a=b=d=e=f=8
1D selection
n·i + (m-1)·a·i
j=64
256
1K
32K
4K
2D selection
l·i + (k-1)·d·i + (j-1)·e·i
1
4
16
64
256
1K
4K
m or k
32M
8M
2M
512K
128K
32K
8K
n or j·l
(n/k)·l + (m-1)·a·l + (k-1)·b·l

FIG. 18B

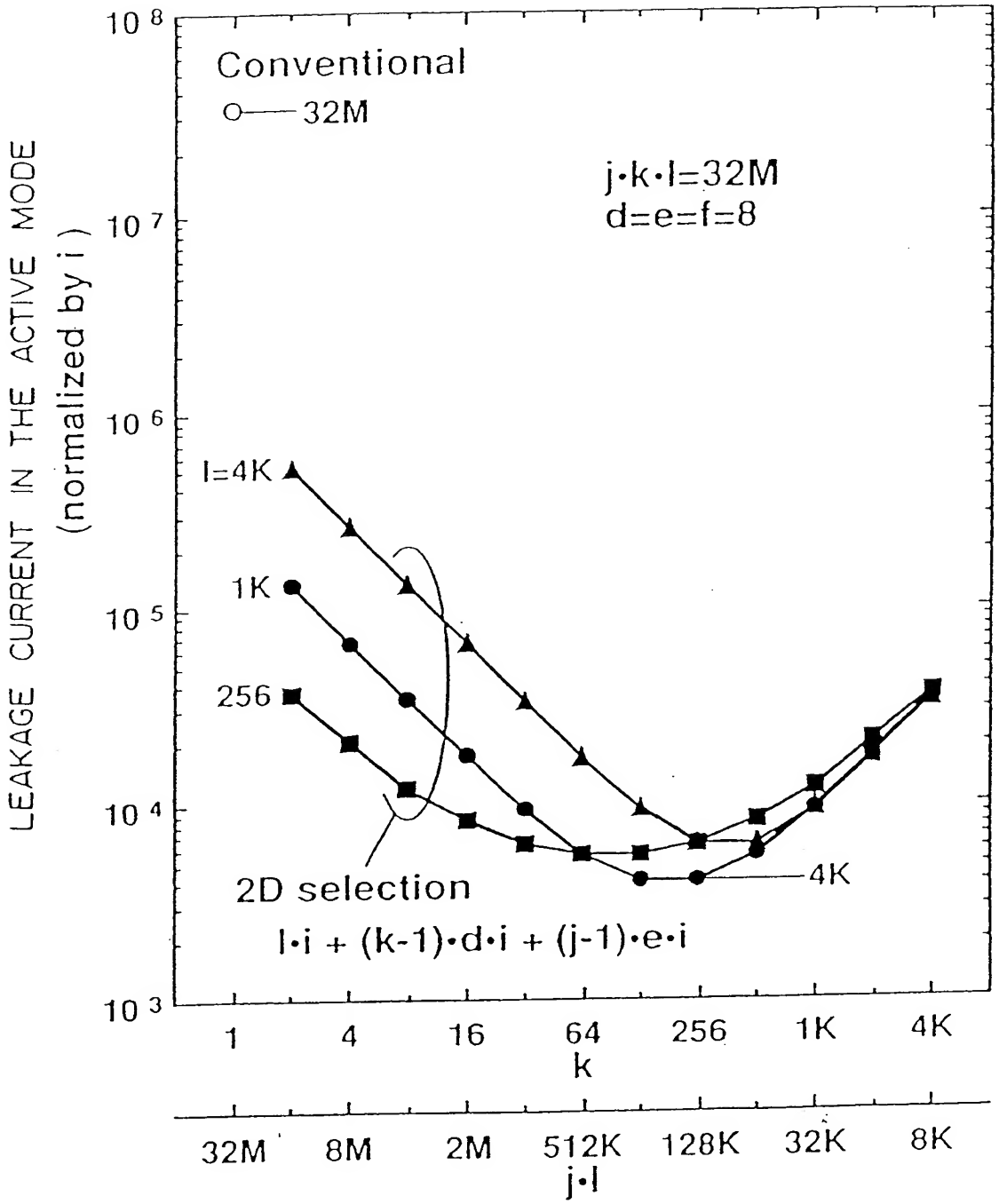

LEAKAGE CURRENT IN THE ACTIVE MODE
(normalized by i)
10 8
10 7
10 6
10 5
10 4
10 3
Conventional
32M
j·k·l=32M
d=e=f=8
l=4K
1K
256
4K
2D selection
l·i + (k-1)·d·i + (j-1)·e·i
1
4
16
64
256
1K
4K
k
32M
8M
2M
512K
128K
32K
8K
j·l

FIG. 19

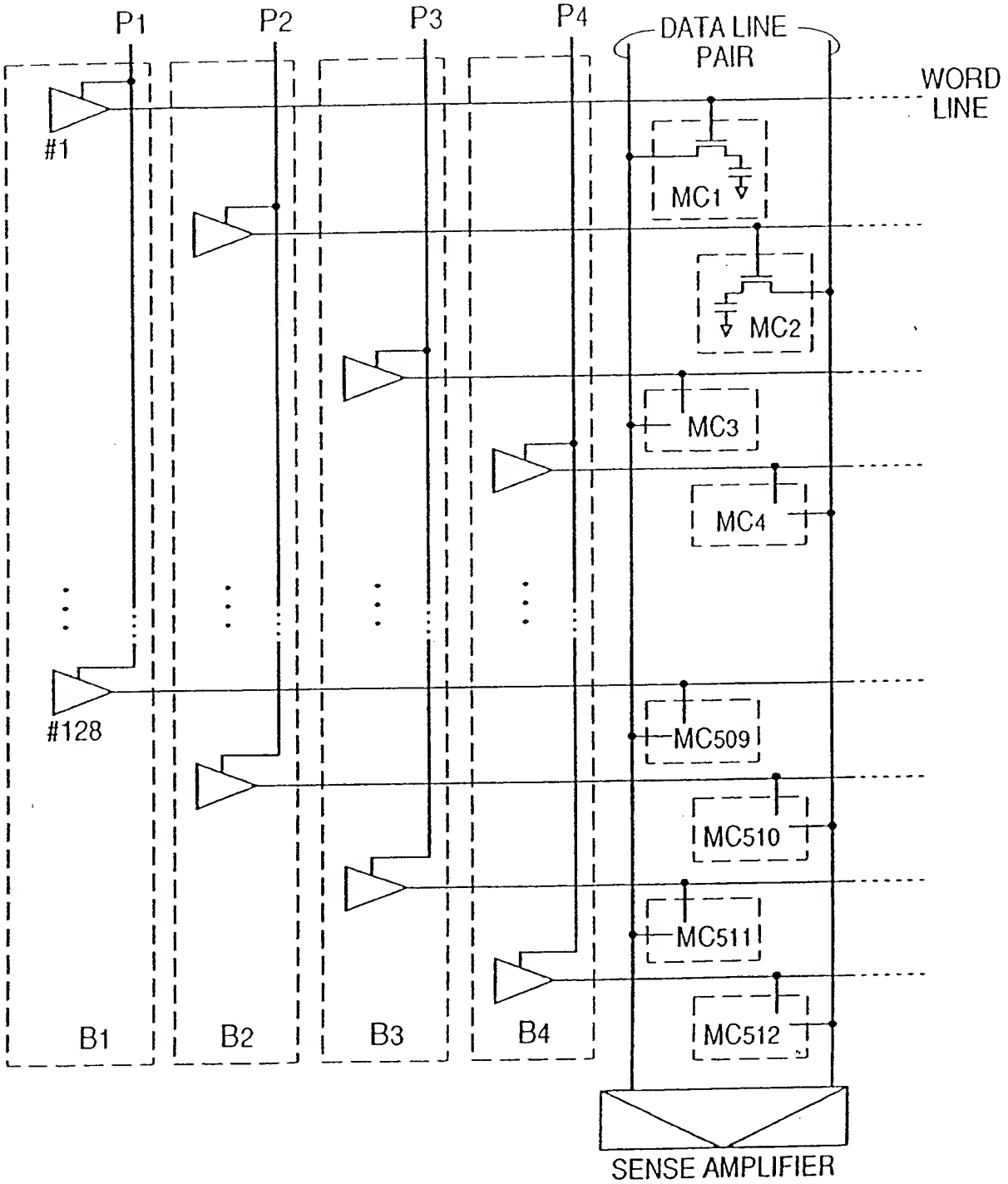

P1
P2
P3
P4
DATA LINE PAIR
WORD LINE
#1
#128
MC1
MC2
MC3
MC4
MC509
MC510
MC511
MC512
B1
B2
B3
B4
SENSE AMPLIFIER

FIG. 20

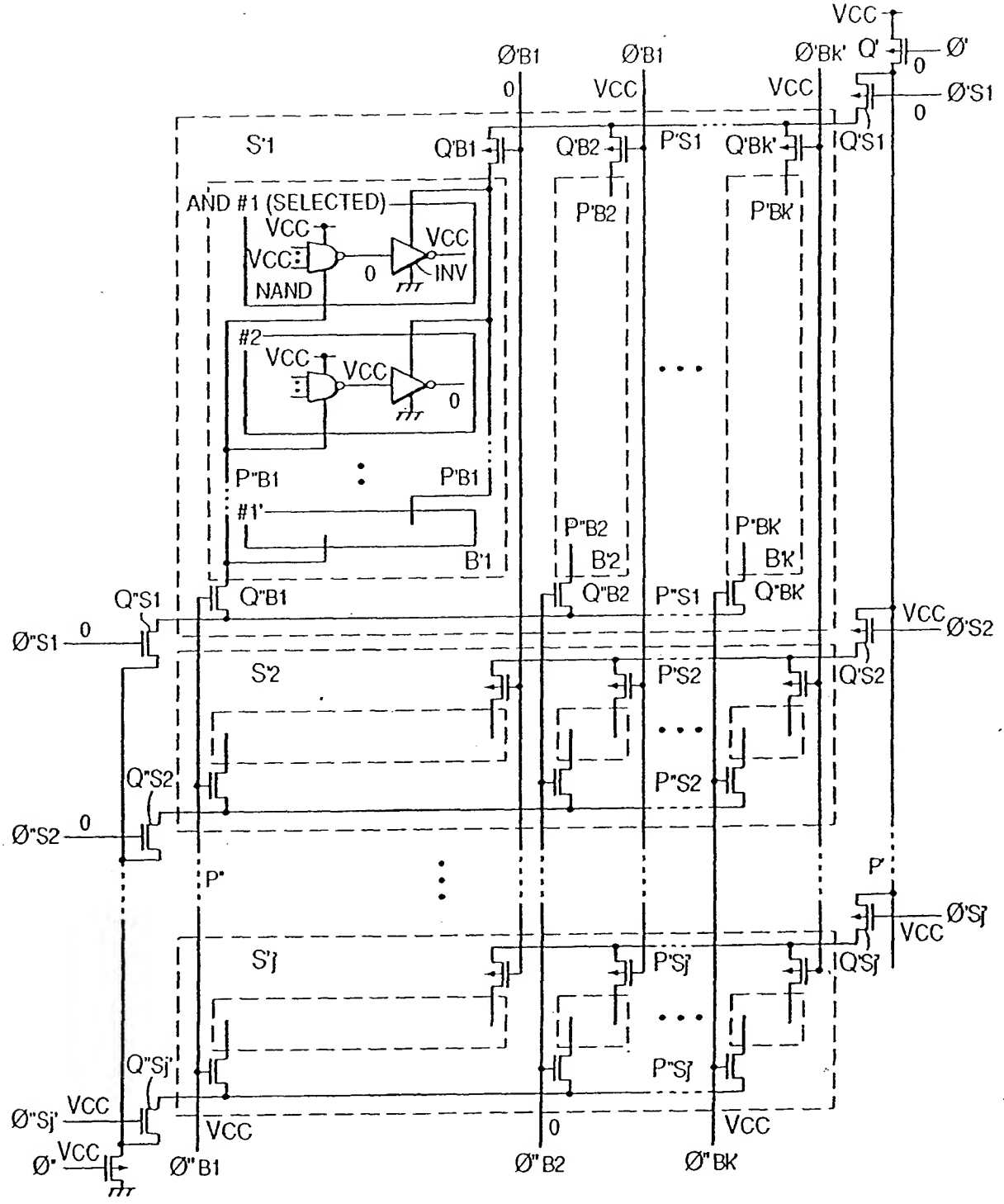

VCC
Ø'B1
Ø'B1
Ø'Bk'
Q'
Ø'
0
VCC
VCC
Ø'S1
0
S'1
Q'B1
Q'B2
P'S1
Q'Bk'
Q'S1
AND #1 (SELECTED)
P'B2
P'Bk'
VCC
VCC
VCC
0
INV
NAND
#2
VCC
VCC
0
P"B1
P'B1
#1'
B'1
P"B2
P"Bk
B'2
B'k
Q"S1
Q"B1
Q"B2
P"S1
Q"Bk
VCC
Ø"S1
0
Ø'S2
S'2
P'S2
Q'S2
Q"S2
P"S2
Ø"S2
0
P"
P'
Ø'Sj
VCC
S'j
P'Sj
Q'Sj
Q"Sj'
P"Sj
Ø"Sj'
VCC
VCC
0
VCC
Ø"
VCC
Ø"B1
Ø"B2
Ø"Bk

FIG. 21

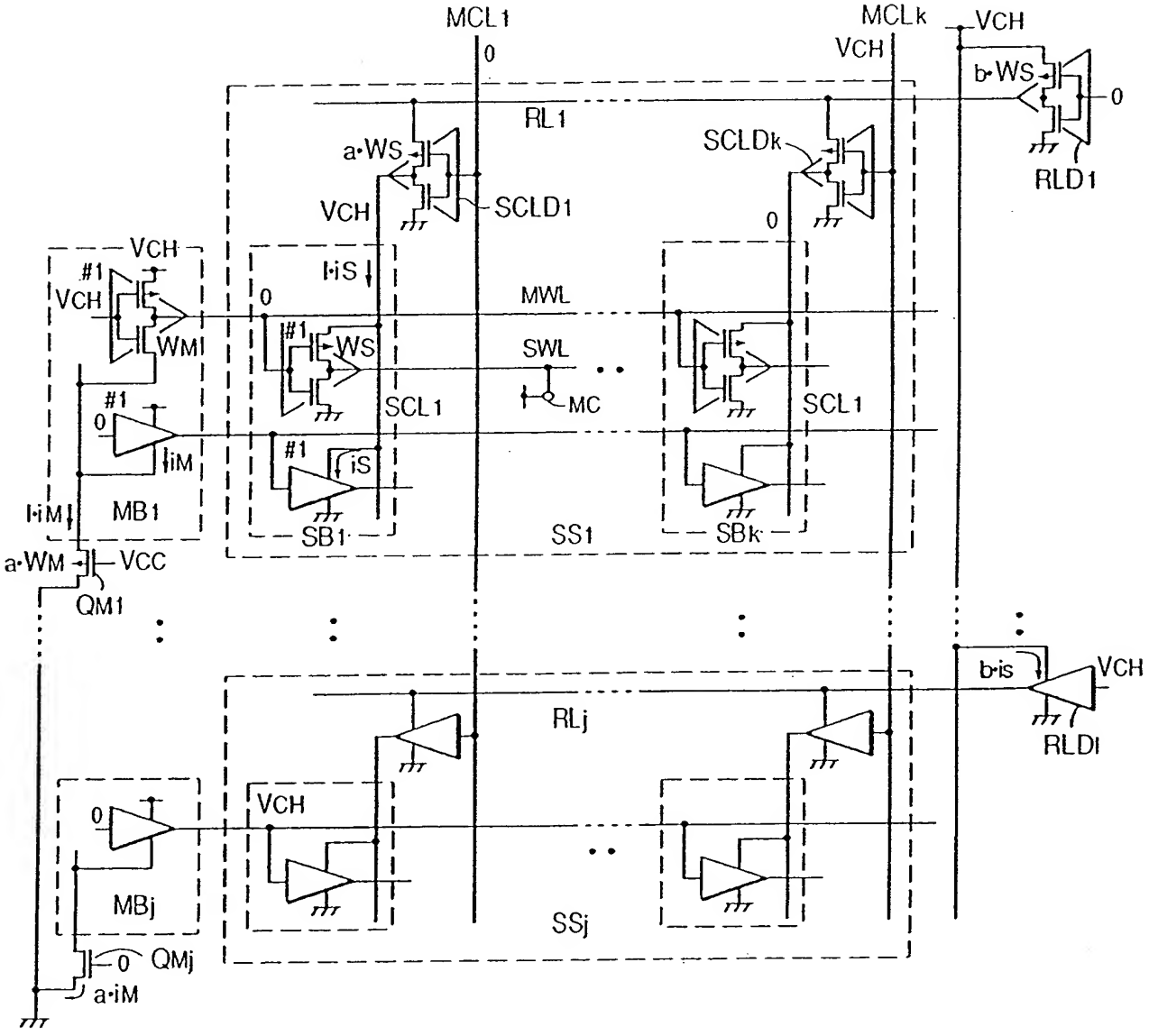

MCL1
MCLk
VCH
RL1
SCLDk
RLD1
a·WS
SCLD1
b·WS
MWL
SWL
MC
SCL1
WM1
WS
iM
iS
MB1
SB1
SS1
SBk
a·WM
VCC
QM1
RLj
RLDj
b·is
MBj
SSj
QMj
a·iM

FIG. 22A
PRIOR ART

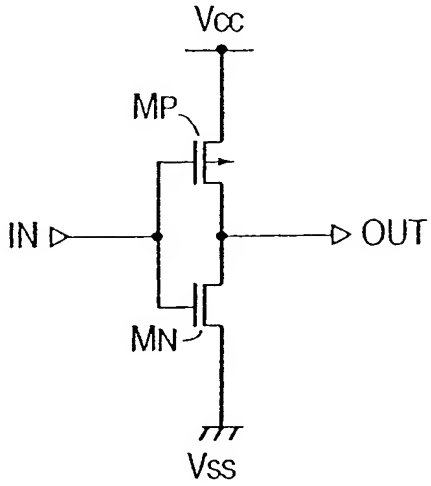


FIG. 22B
PRIOR ART

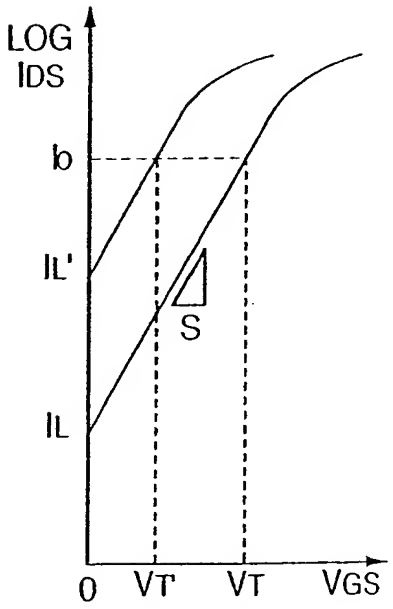


FIG. 23
PRIOR ART

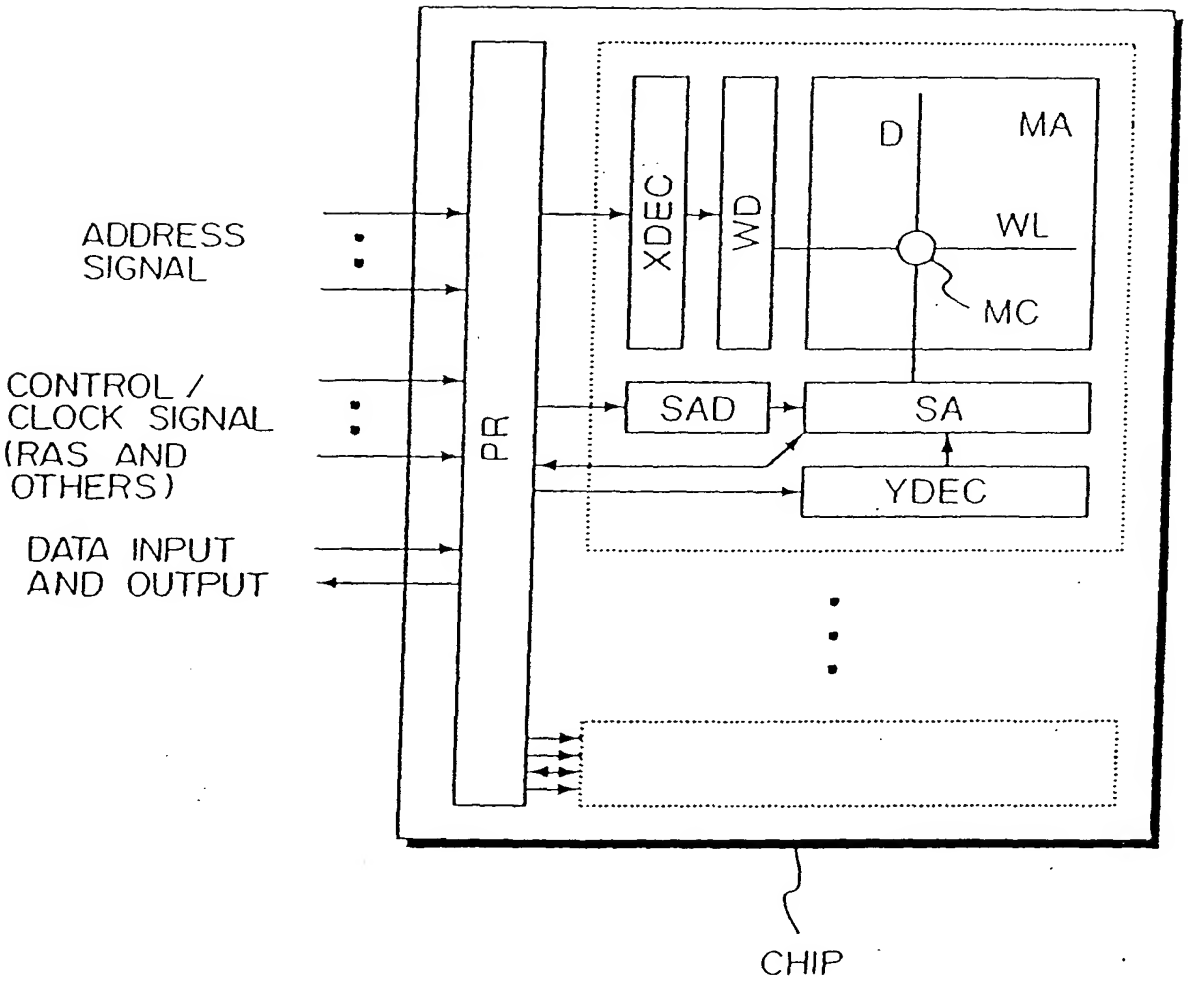


FIG. 24
PRIOR ART

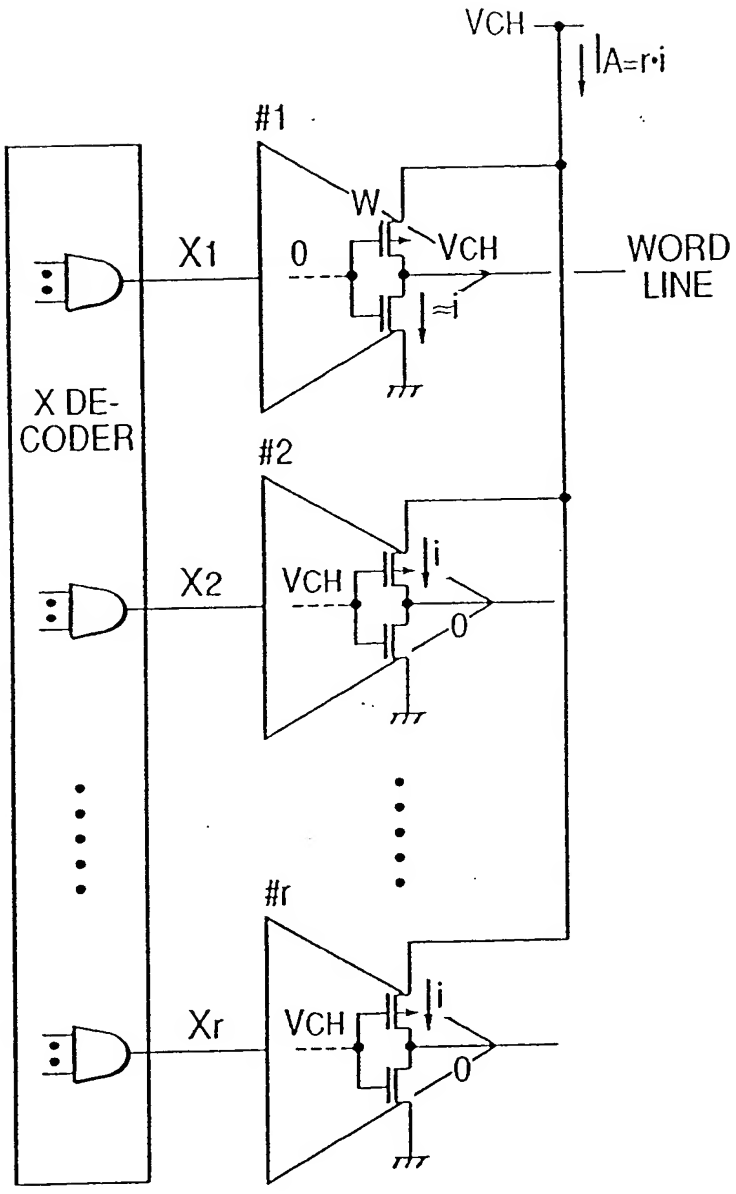
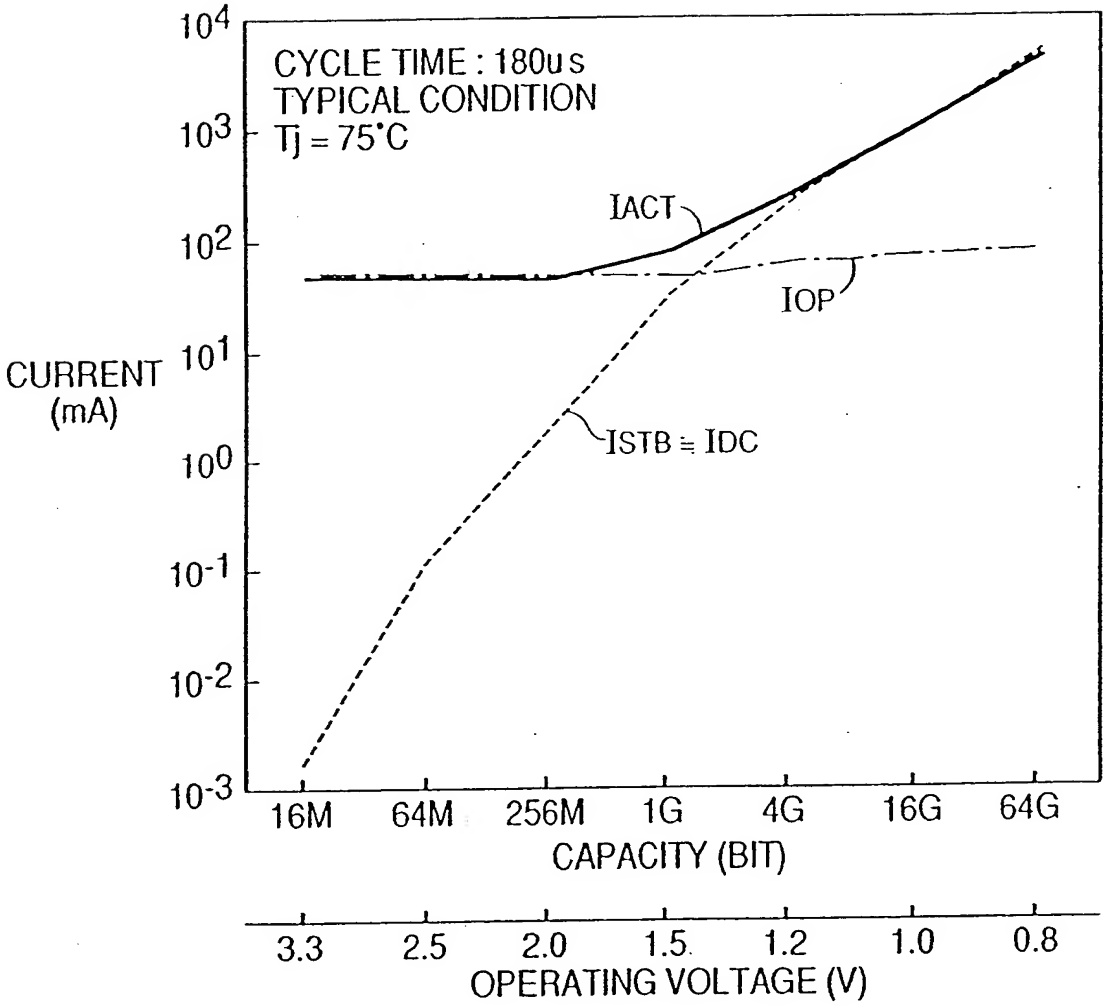


FIG. 25


CYCLE TIME : 180u s
TYPICAL CONDITION
Tj = 75°C
IACT
IOP
ISTB ≒ IDC
CURRENT (mA)
10^4
10^3
10^2
10^1
10^0
10^-1
10^-2
10^-3
16M
64M
256M
1G
4G
16G
64G
CAPACITY (BIT)
3.3
2.5
2.0
1.5
1.2
1.0
0.8
OPERATING VOLTAGE (V)